



SEMiSTART

Antiparallel thyristors for softstart

SKKQ 1500/18E

Features

- Compact design
- Thyristor with amplifying gate
- Pressure contact technology

Typical Applications*

- Soft starters

Remarks

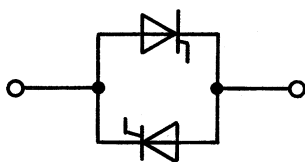
- Please note: This module has no soft mold protection around the chip. It is therefore susceptible to environmental influences (dust, humidity, etc.). The humidity test according to IEC60068-2-67 is not passed by this product.
- Recommendation: The devices should be installed in control cabinets of IP54 degree of protection.

Footnotes

¹⁾ T_{jmax} up to 150°C is allowable for overload conditions, max. time period for the overload condition is 20s.

Absolute Maximum Ratings				
Symbol	Conditions	Values	Unit	
Module				
$I_{overload}$	W1C, sin. 180°, 20 s, $T_{jmax} = 150\text{ °C}$, $T_{jstart} = 40\text{ °C}$	1500	A	
I_{TSM}	10 ms	$T_j = 25\text{ °C}$	17000	A
		$T_j = 125\text{ °C}$	15000	A
i^2t	10 ms	$T_j = 25\text{ °C}$	1445000	A ² s
		$T_j = 125\text{ °C}$	1125000	A ² s
V_{RSM}		1900	V	
V_{RRM} V_{DRM}		1800	V	
T_j	¹⁾	-40 ... + 125	°C	
T_{stg}		-40 ... + 125	°C	

Characteristics					
Symbol	Conditions	min.	typ.	max.	Unit
V_T	$T_j = 25\text{ °C}$, $I_T = 1700\text{ A}$			1.5	V
$V_{T(TO)}$	$T_j = 125\text{ °C}$			0.85	V
r_T	$T_j = 125\text{ °C}$			0.3	mΩ
$I_{DD}; I_{RD}$	$T_j = 125\text{ °C}$, $V_{RD} = V_{RRM}$, per module			190	mA
t_{gd}	$T_j = 25\text{ °C}$, $I_G = 1\text{ A}$, $di_G/dt = 1\text{ A}/\mu\text{s}$		1		μs
t_{gr}	$V_D = 0.67 \cdot V_{DRM}$		2		μs
$(dv/dt)_{cr}$	$T_j = 125\text{ °C}$		1000		V/μs
$(di/dt)_{cr}$	$T_j = 125\text{ °C}$, $f = 50 \dots 60\text{ Hz}$		200		A/μs
t_q	$T_j = 125\text{ °C}$		200		μs
I_H	$T_j = 25\text{ °C}$		150	500	mA
I_L	$T_j = 25\text{ °C}$, $R_G = 33\text{ Ω}$		300	2000	mA
V_{GT}	$T_j = 25\text{ °C}$, d.c.	3			V
I_{GT}	$T_j = 25\text{ °C}$, d.c.	200			mA
V_{GD}	$T_j = 125\text{ °C}$, d.c.			0.25	V
I_{GD}	$T_j = 125\text{ °C}$, d.c.			10	mA
$R_{th(j-r)}$	continuous DC, per thyristor			0.037	K/W
M_t	to terminals	4.25		5.75	Nm
m	approx.		1200		g
Case			2		



W1C

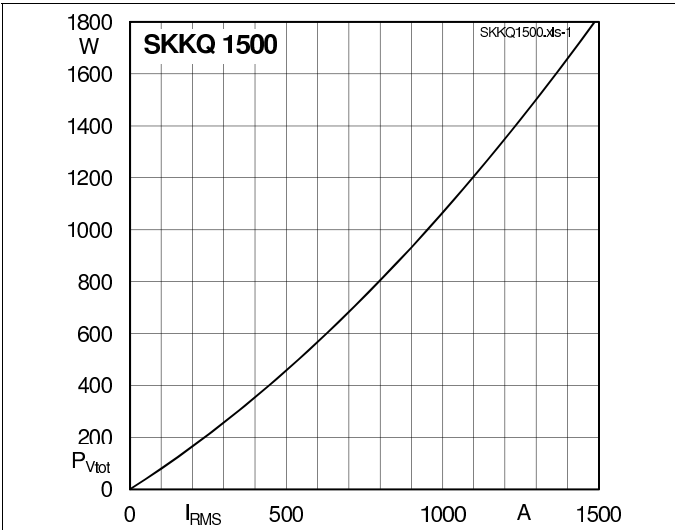


Fig. 1: Power dissipation per module vs. rms current

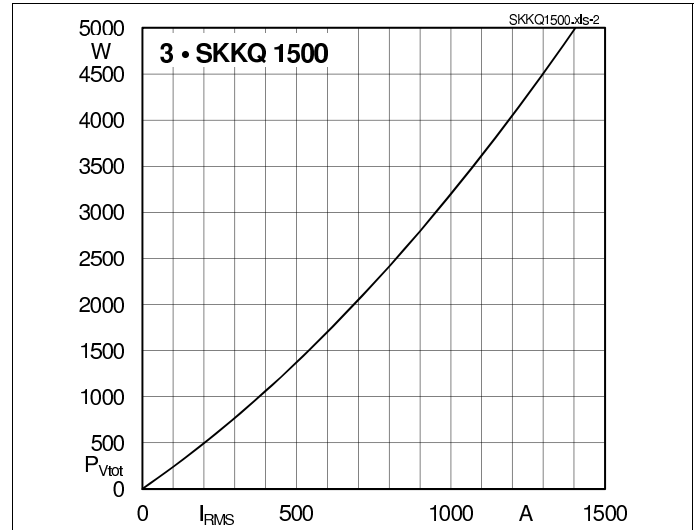


Fig. 2: Power dissipation of three modules vs. rms current

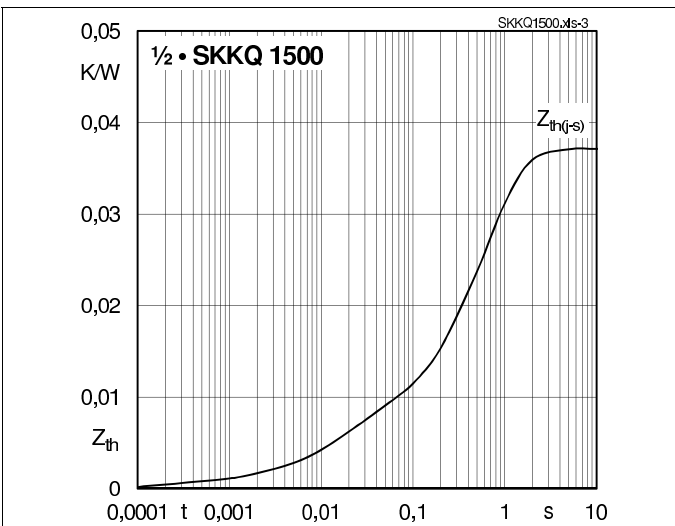


Fig. 3: Transient thermal impedance $Z_{th(j-r)}$ vs. time

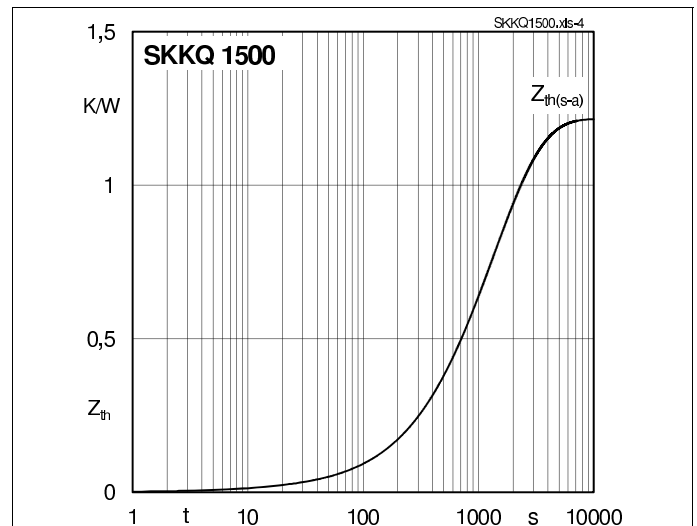


Fig. 4: Typ. transient thermal impedance $Z_{th(s-a)}$ vs. time (natural cooling)

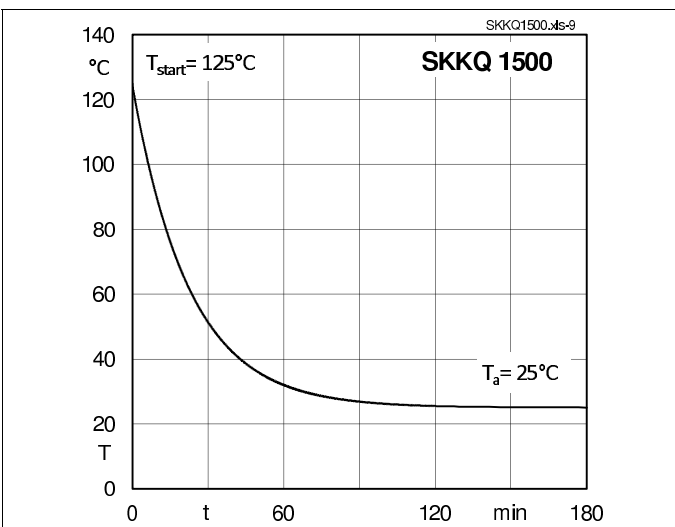


Fig. 5: Typ. cooling down vs. time (natural cooling)

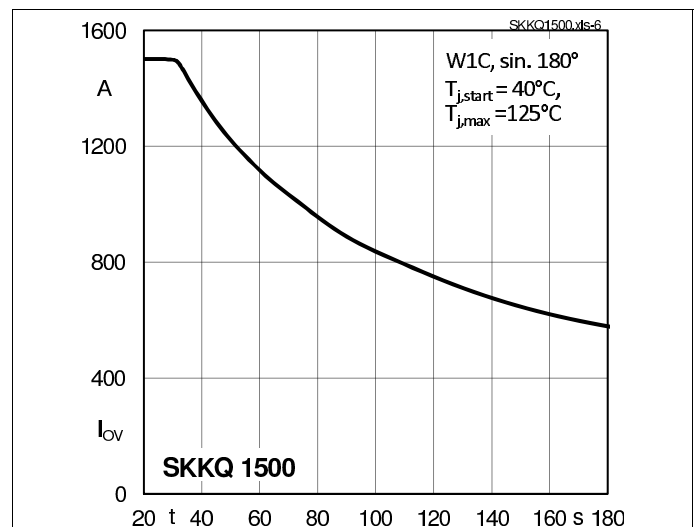


Fig. 6: Typ. overload current vs. time (natural cooling)

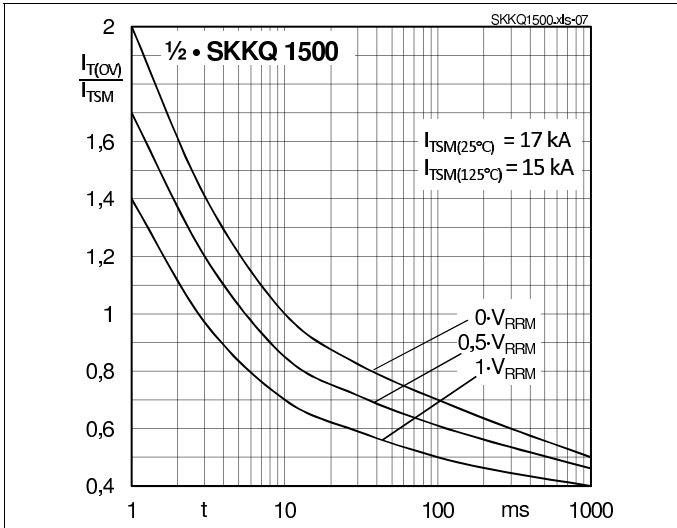


Fig. 7: Surge overload current vs. time

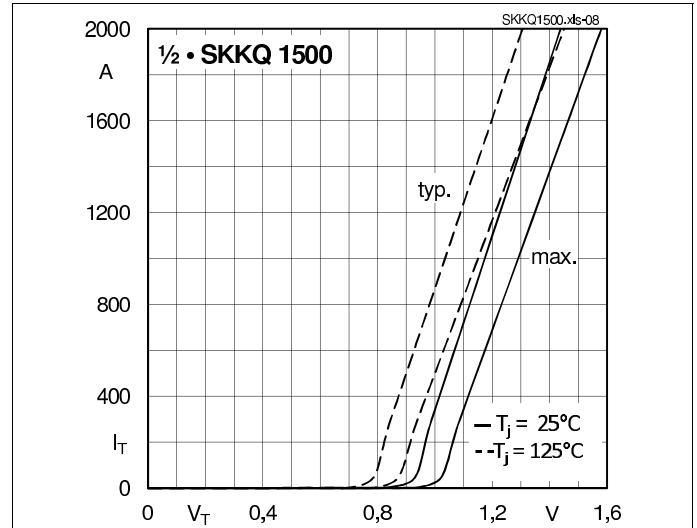


Fig. 8: On state characteristics

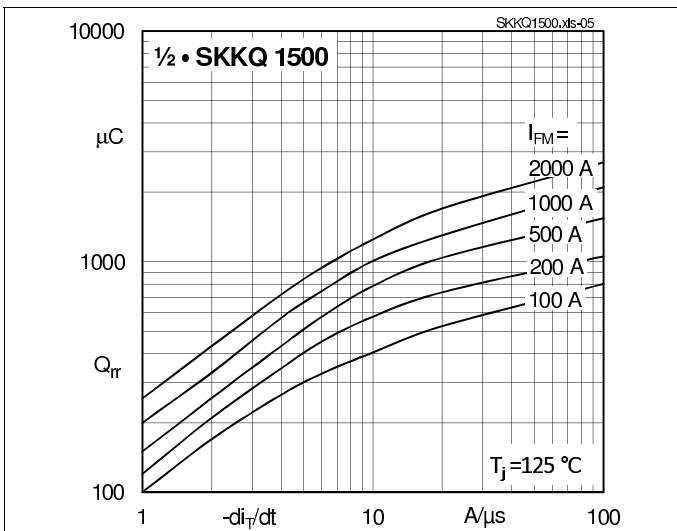


Fig. 9: Recovery charge vs. current decrease

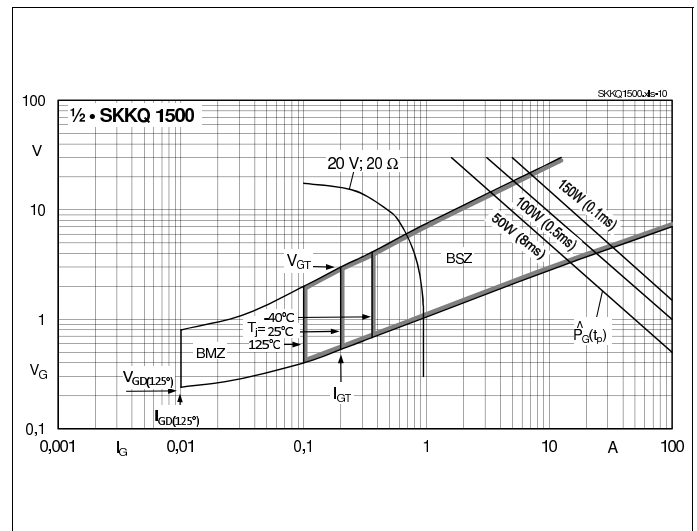
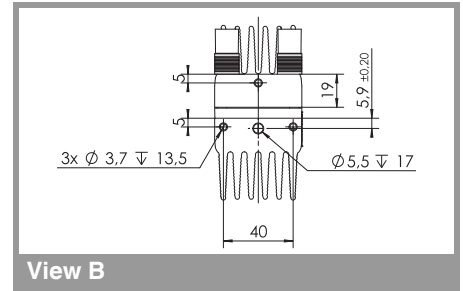
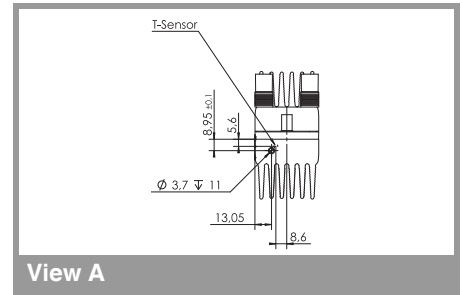
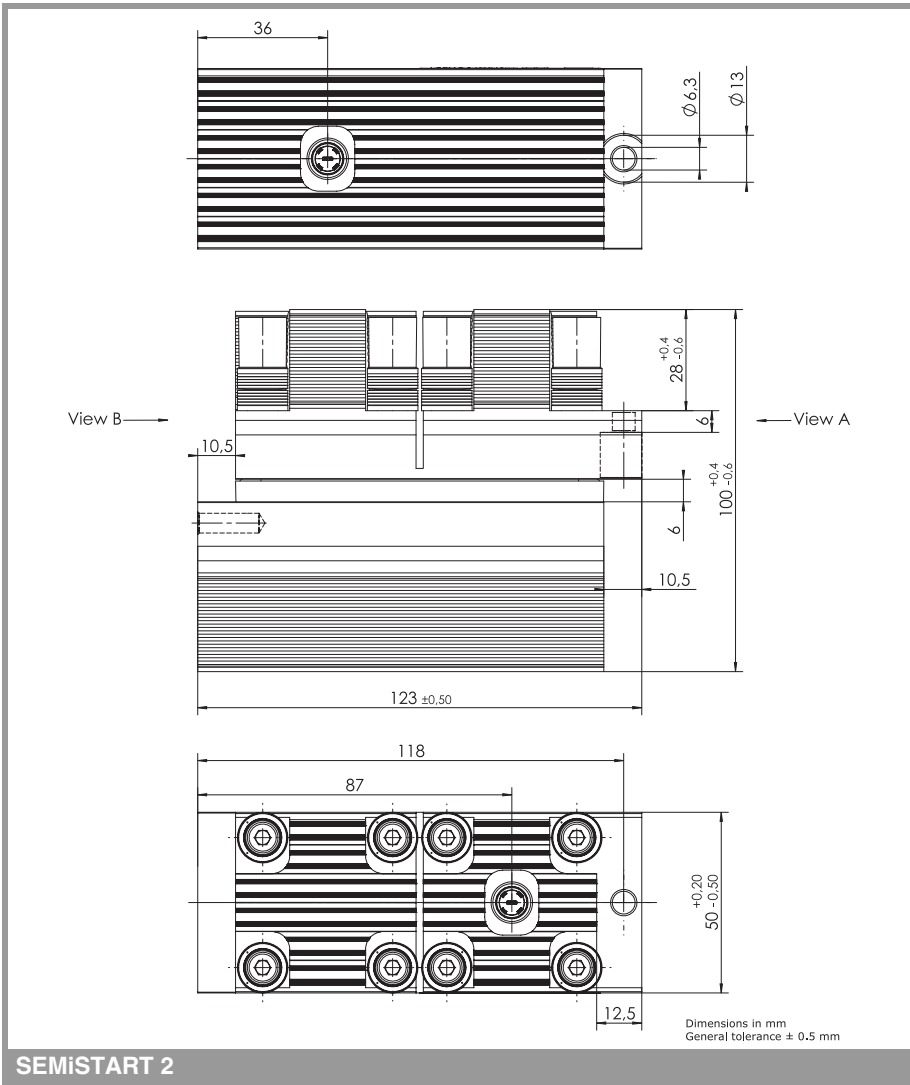


Fig. 10: Gate trigger characteristic

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This is an electrostatic discharge sensitive device (ESDS), international standard IEC 60747-1, chapter IX.

*IMPORTANT INFORMATION AND WARNINGS

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